

Arquitectura de Computadores

CC4301

Clase 6: Diseño Modular

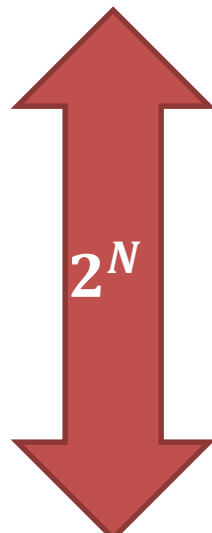
Semestre Primavera 2013
Profesor: Pablo Guerrero

Motivación

tabla de verdad: filas = 2^N

⇒ Metodología no sirve
para muchas entradas!

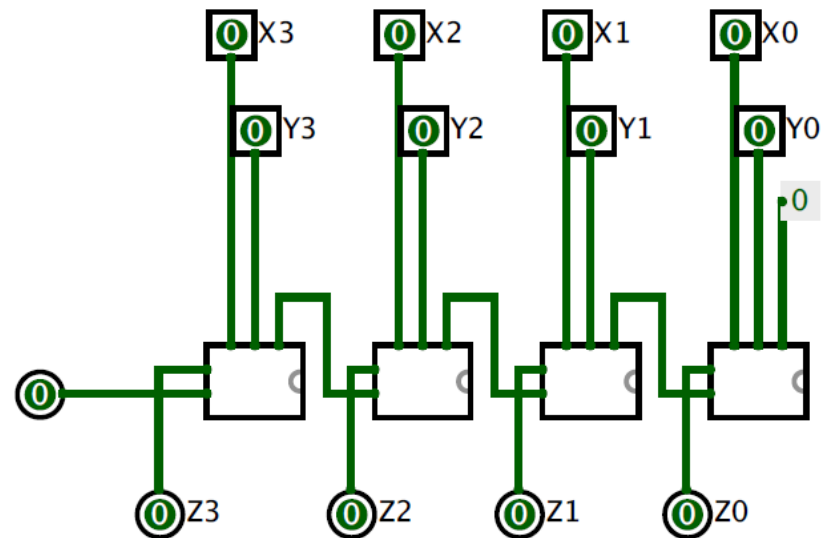
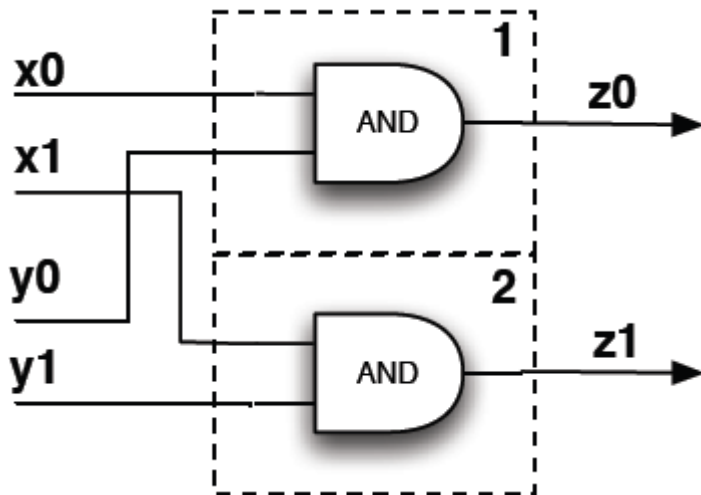
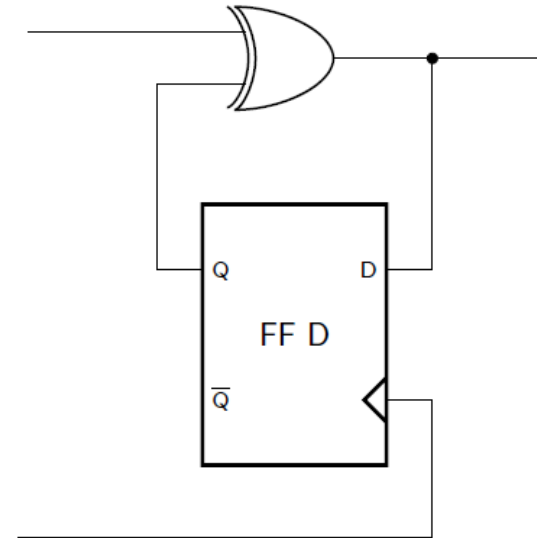
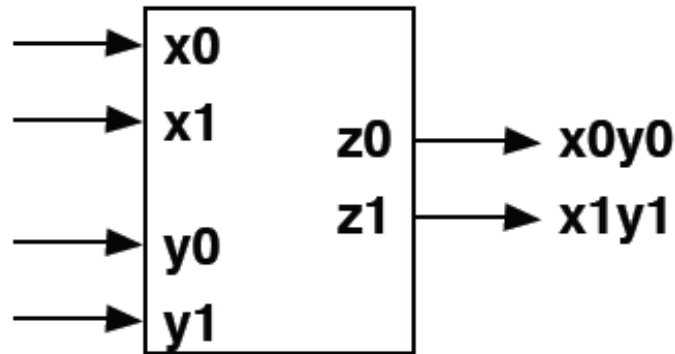
Mejor acoplar circuitos más
simples ⇒ **Diseño Modular**



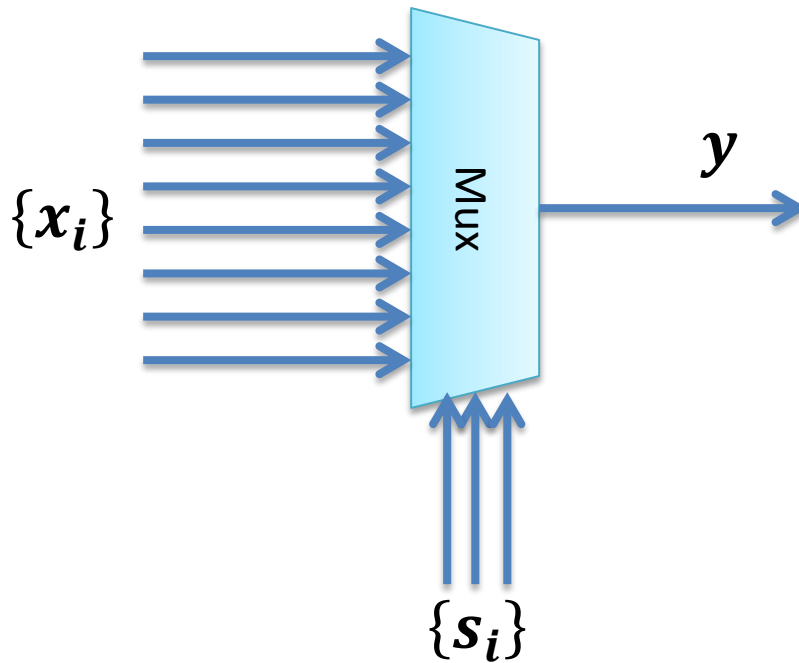
x_2	x_1	x_0	d_1	d_0	y
0	0	0	1	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	1	0	1
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	0	1

Estrategias

- Paralelo
- Cascada
- Serial o Secuencial

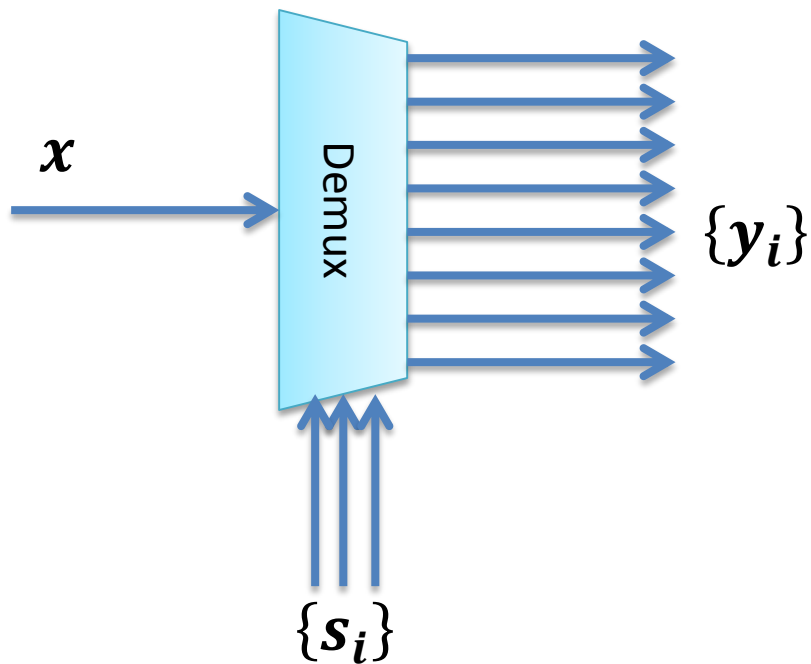


Multiplexor (Mux)



s	x_1	x_0	y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

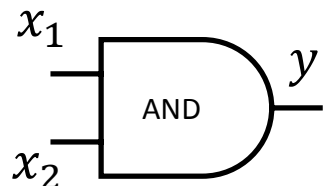
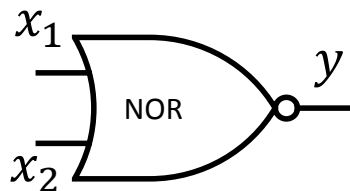
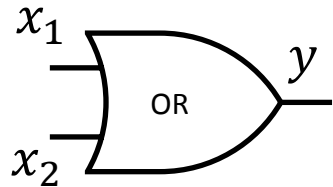
Demultiplexor (Demux)



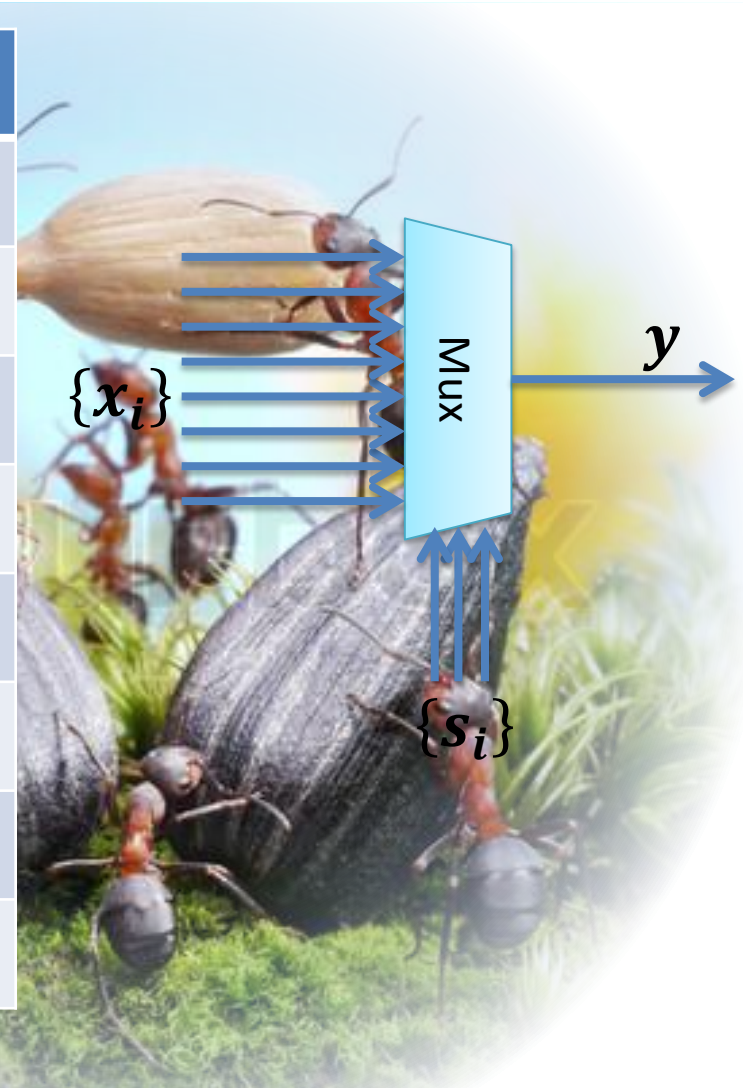
s	x	y_0	y_1
0	0	0	0
0	1	1	0
1	0	0	0
1	1	0	1

Trabajo Grupal 1

- Recordar:

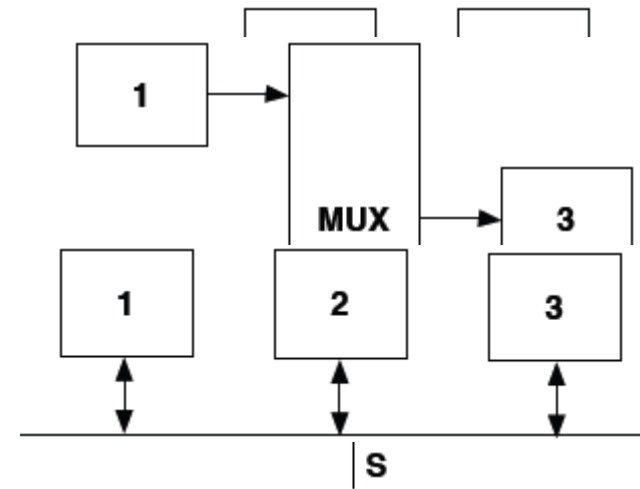


s	x_1	x_0	y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

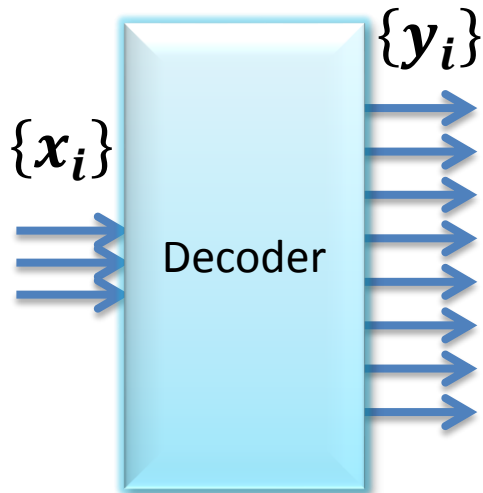


Estrategias de Comunicación

- Punto a punto
- 1 a N
- N a 1
- Bus



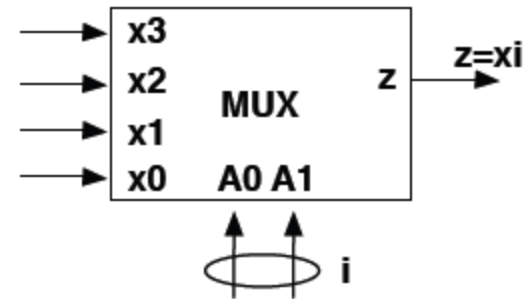
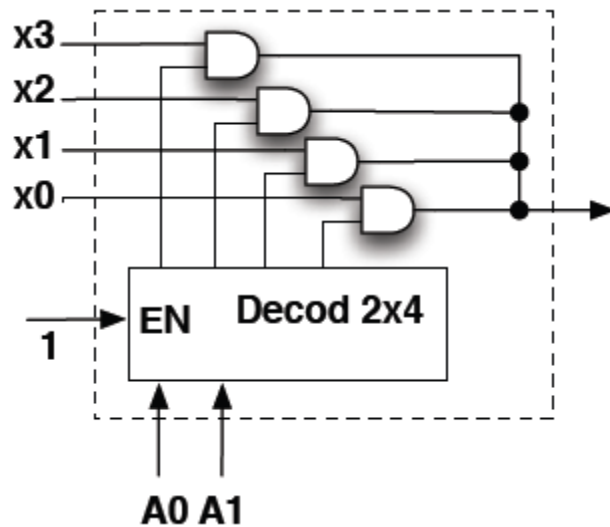
Decodificador (Decoder)



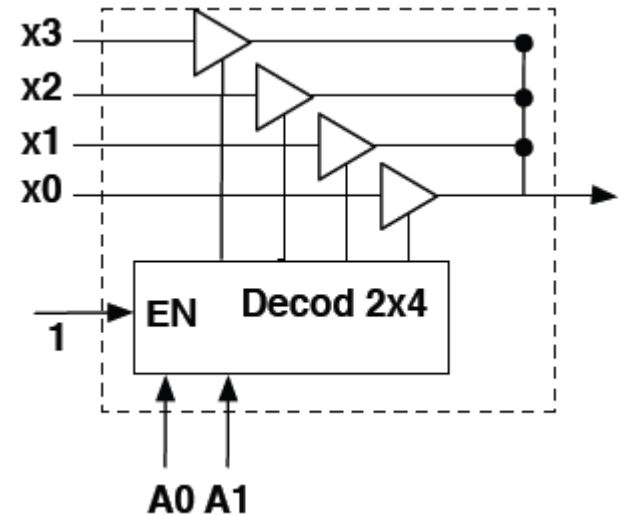
x_2	x_1	x_0	y_7	y_6	y_5	y_4	y_3	y_2	y_1	y_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Implementación Multiplexor

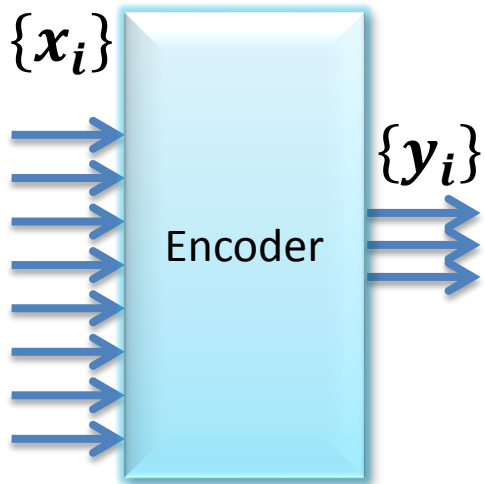
- Usando AND:



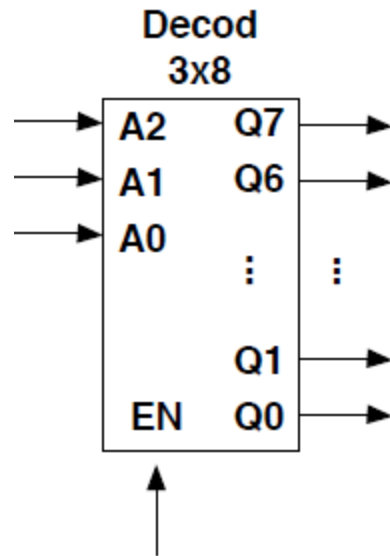
- tas tristate:



Codificador (Encoder)

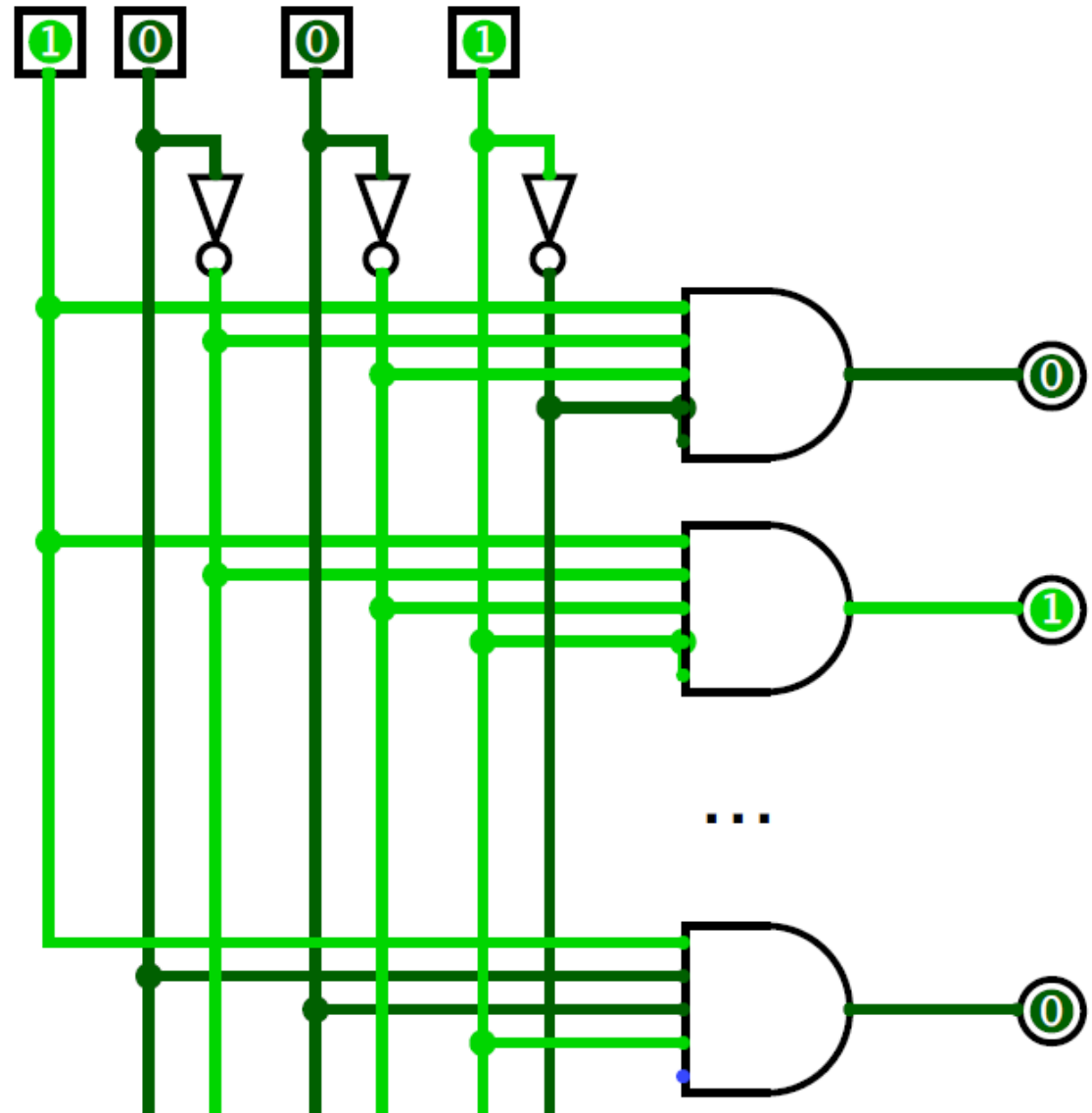
[illegible]

Implementación Decodificador



$i = A2...A0$

$$Q_j = \begin{cases} 0 & \text{si } EN = 0 \\ 0 & \text{si } i \neq j, EN = 1 \\ 1 & \text{si } i = j, EN = 1 \end{cases}$$



Decodificador 6x64

9 Decod 3x8 en cascada y/o paralelo

