Introduction to ASIC Design

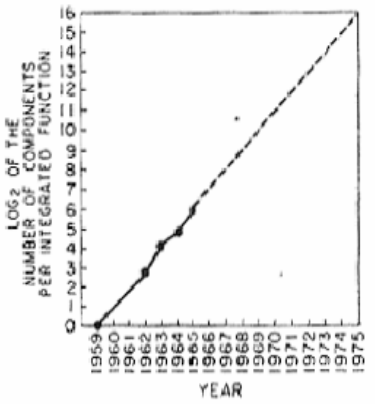
Outline

1. The wonderful world of Silicon
2. Application Specific Integrated Circuits (ASICs)
   - Typical applications, types, decision making
3. ASIC Design Flow
4. Trends

The Wonderful World of Silicon

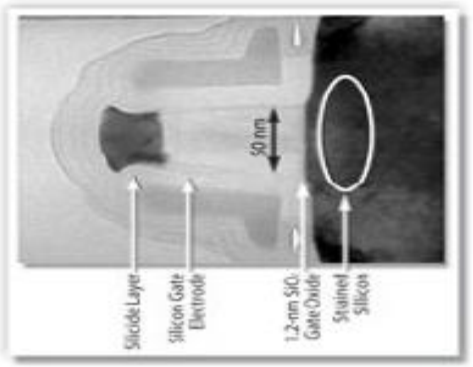
“Moores Law”

- About every eighteen months, the number of transistors on a CMOS silicon chip doubles and the clock speed doubles
  - Transistors/Chip increasing by 50% per year (by 4× in 3.5 years)
  - Gate Delay decreasing by 13% per year (by ½ in 5 years)
- This rate of improvement will continue until about 2018 at least.



Technology Drivers

- Decreasing lithographic feature size, e.g. measured by the transistor gate length:
  - 0.13 µm, 0.090 µm, 0.065 µm, … 0.01 µm(?)
- Increasing wafer size:
  - 8 inch diameter….. 12 in.
- Increasing number of metal interconnect layers:
  - 6 ….. 8 …… 9 ….



Cost Scaling

- Cost per transistor scales down:
  - Approximately constant cost per wafer to manufacture:
  - About $2,000 - $4,000 per wafer
  - Increasing IC yields for ‘large’ (> 1 sq. cm.chips): 60% …. 90%
- But cost to first chip scales up!
  - Design cost increases with transistor count
  - Mask cost increases with each new family

Semiconductor Roadmap

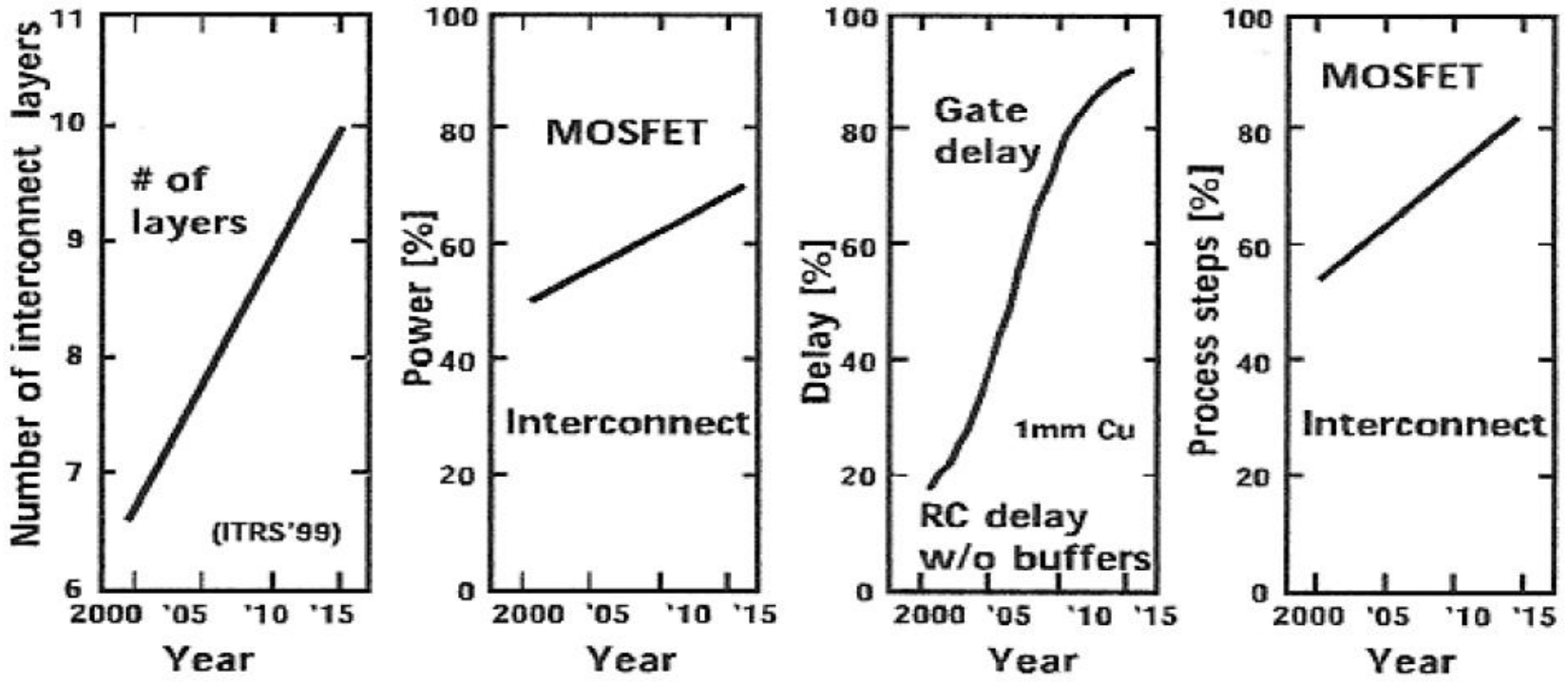
Projections for 'leading edge' ASIC/MPU: (www.itrs.net)

Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
ASIC									
ASIC usable Mtransistors/cm^2 (auto layout)	225	283	357	449	566	714	899	1,133	1,427
ASIC max chip size at production (mm^2) (maximum lithographic field size)	*858*	*858*	*858*	*858*	*858*	*858*	*858*	*858*	*858*
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	1,928	2,430	3,061	3,857	4,859	6,122	7,713	9,718	12,244
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	44.0	31.1	22.0	15.6	11.0	7.8	5.5	3.9	2.8
Chip Frequency (MHz)									
On-chip local clock [1]	5,204	6,783	9,285	10,972	12,369	15,079	17,658	20,065	22,980
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[2]	3,125	3,906	4,883	6,103	7,629	9,536	11,920	14,900	18,625
Maximum number wiring levels—maximum [3]	15	15	15	16	16	16	16	16	17
Maximum number wiring levels—minimum [3]	11	11	11	12	12	12	12	12	13

Other Scaling Trends

The impact of the wiring increases with each generation



ASICs vs. What?

Application Specific Integrated Circuit

- A chip designed to perform a particular operation as opposed to General Purpose integrated circuits
- An ASIC is generally NOT software programmable to perform a wide variety of different tasks

An ASIC will often have an embedded CPU to manage suitable tasks

An ASIC may be implemented as an FPGA (see later)

- Sometimes considered a separate category

ASICs vs. What? (contd.)

General Purpose Integrated Circuits:

Examples:

- Programmable microprocessors (e.g. Intel Pentium Series, Motorola HC-11)
  - Used in PCs to washing machines
  - Programmable Digital Signal Processors (e.g. TI TMS 320 Series)
- Used in many multimedia, sensor processing and communications applications
  - Memory (dRAM, SRAM, etc.)

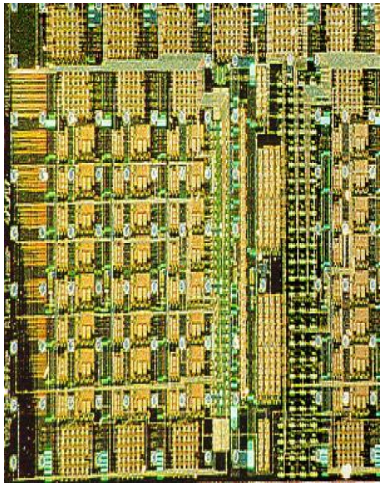
Examples of ASICs

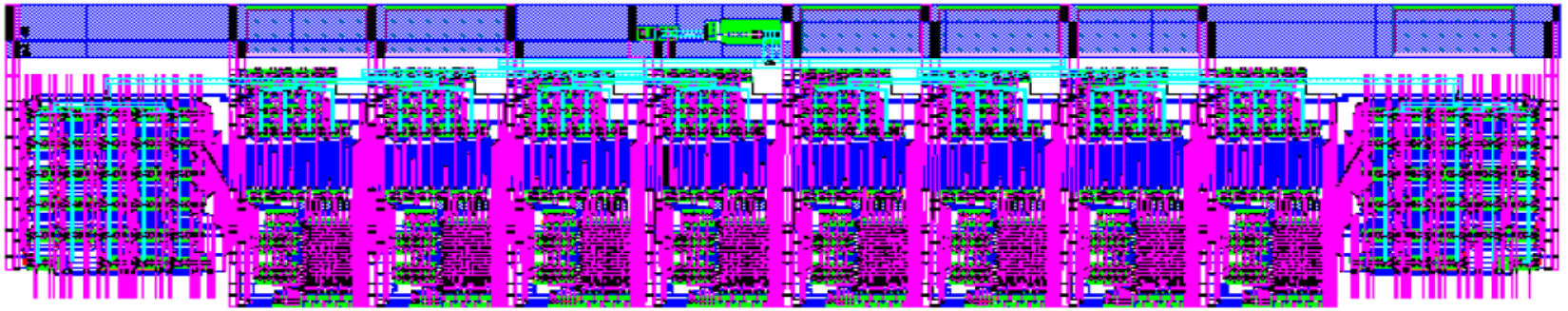
- Video processor to decode or encode MPEG-2 digital TV signals
- Low power dedicated DSP/controller /convergence device for mobile phones
- Encryption processor for security
- Many examples of graphics chips
- Network processor for managing packets, traffic flow, etc.

ASIC Styles

Full Custom ASICs

- Every transistor is designed and drawn by Hand
- Typically only way to design analog portions of ASICs
- Gives the highest performance but the longest design time
- Full set of masks required for fabrication

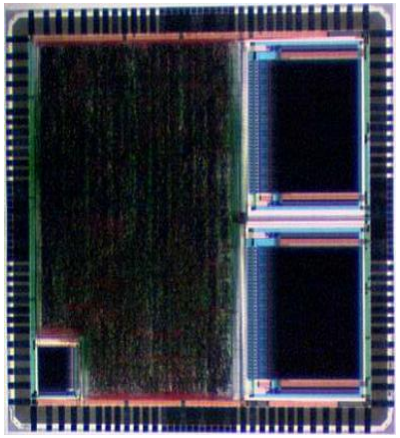




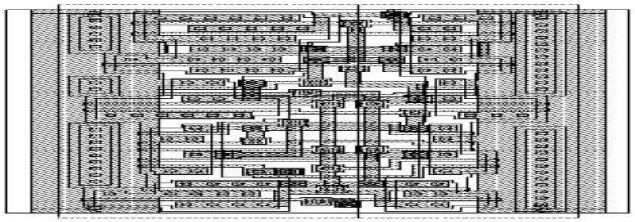
ASIC Styles (Contd.)

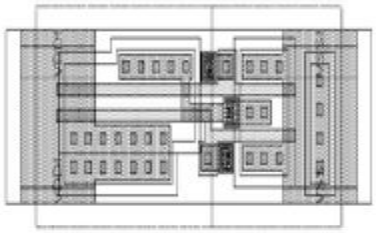
Standard-Cell-Based ASICs

- or ‘Cell Based IC’ (CBIC) or ‘semi-custom’
- **Standard Cells are custom designed and then inserted** into a **library**
- These cells are then used in the design by being placed in rows and wired together using ‘place and route’ CAD tools
- Some standard cells, such as RAM and ROM cells, and some datapath cells (e.g. a multiplier) are tiled together to create **macrocells**



D-flip-flop:



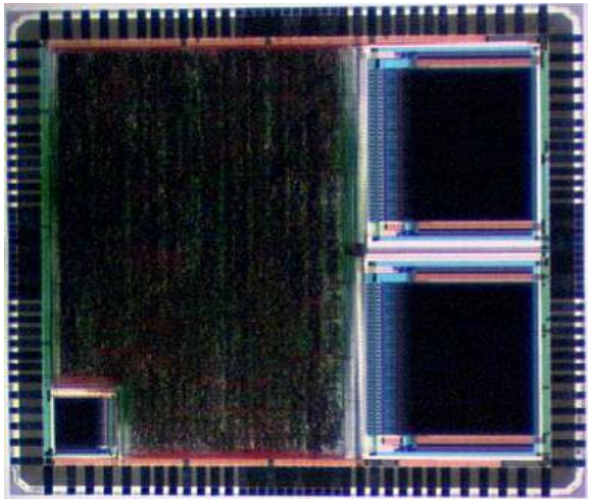


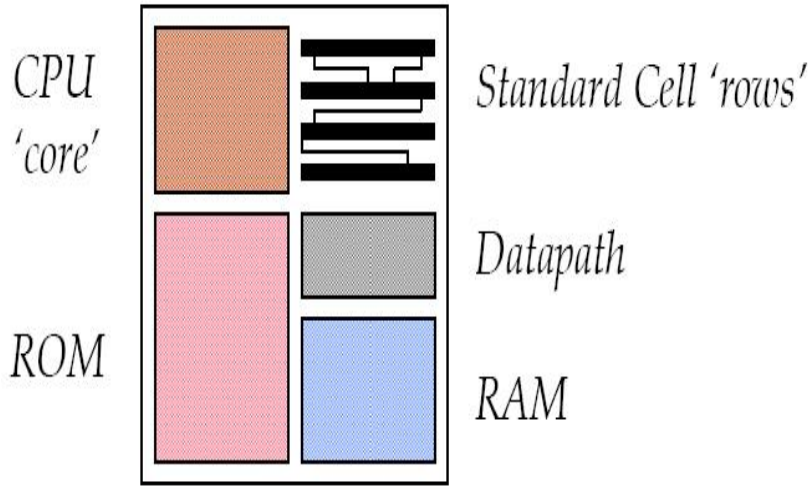
NOR gate:

Standard Cell ASICs (cont'd)

Sample ASIC floorplan:

- Standard Cell designs are usually synthesized from an RTL (Register Transfer Language) description of the design
- Full set of masks (22+) still required





Cell based ASICs (cont'd)

Fabless semiconductor company model

- Company does design only. Fab performed by another company (e.g. TSMC, UMC, IBM, Philips, LSI).
- Back-end (place and route, etc.) might be performed at that company or with their assistance

ASIC Styles (cont'd)

Gate-Array Based ASICs

- In a gate array, the transistors level masks are fully defined and the designer can not change them
- The design instead programs the wiring and vias to implement the desired function
- Gate array designs are slower than cell-based designs but the implementation time is faster as less time must be spent in the factory
- RTL-based methods and synthesis, together with other CAD tools, are often used for gate arrays.

Gate Array (cont'd)

Examples:

Chip Express

- Wafers built with sea of macros + 4 metal layers
- 2 metal layers customized for application
- Only 4 masks!

Triad Semiconductor

- Analog and Digital Macros
- 1 metal layer for customization (2 week turnaround)

ASIC Styles (cont'd)

Programmable Logic Devices (PLDs and FPGAs)

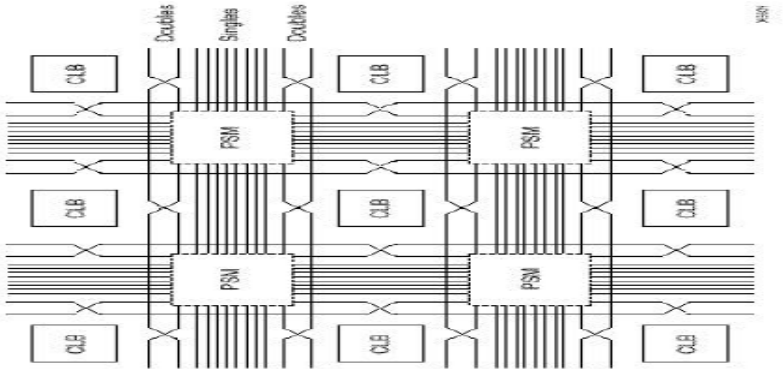
- FPGA= Field Programmable Gate Array
- Are off-the-shelf ICs that can be programmed by the user to capture the logic
- There are no custom mask layers so final design implementation is a few hours instead of a few weeks
- Simple PLDs are used for simple functions.
- FPGAs are increasingly displacing standard cell designs.
- Capable of capturing 100,000+ designed gates
- High power consumption
- High per-unit cost

FPGA (cont'd)

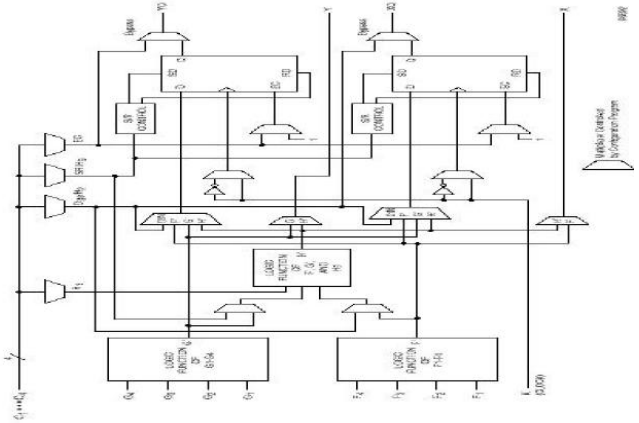
Sample internal architecture:

- Store logic in look-up table (RAM)
- Programmable interconnect

Programmable Interconnect Array:



Configurable Logic Block (CLB):

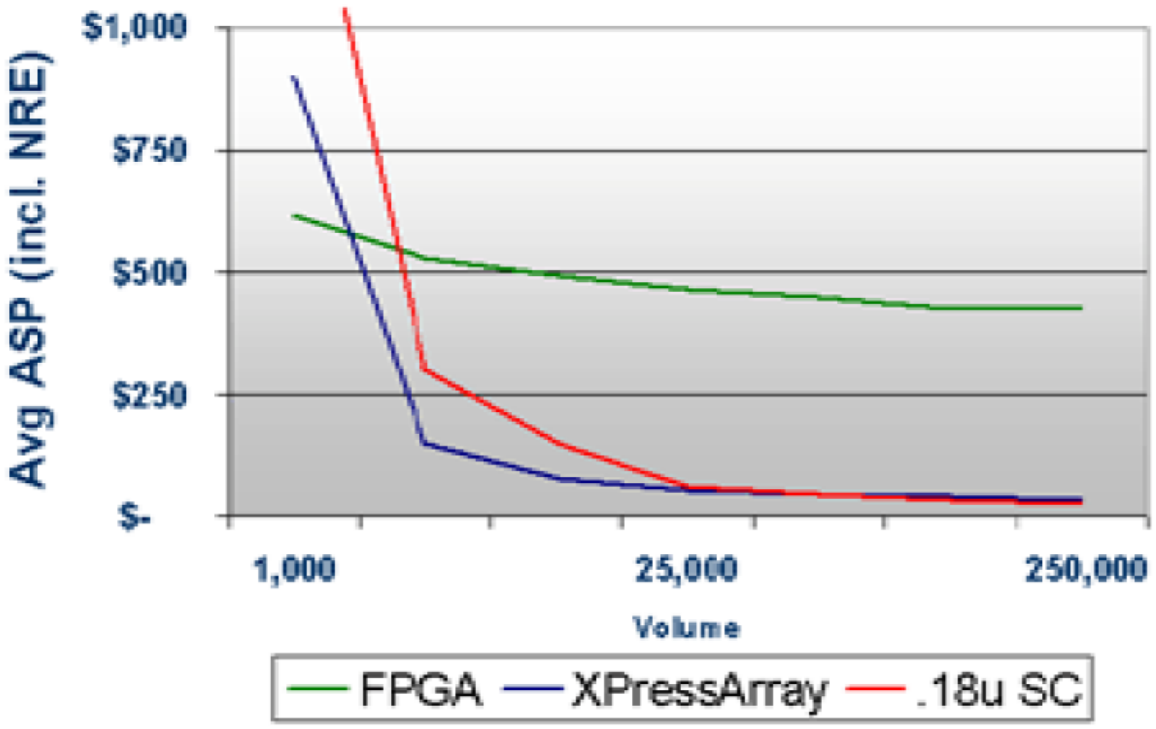


FPGA (cont'd)

	uProc or DSP	FPGA	Gate Array	Standard Cell
Positives:	Lowest NRE cost Fast Time to Market	Low NRE Fast Time to Market	Reasonable NRE & time to market Moderate Performance (~1M gates @ 200 MHz) Good pricing (<$10)	Highest Performance (10 M gates @ 500+ MHz) Lowest volume cost. Low power consumption
Negatives:	Lowest Performance Highest Power Consumption	Low Performance (10k – 1M ==gates @ 10 –100 MHz) High power consumption High recurring cost ($1 - $1,000)		High Design and Mask costs ($10M+). Long time to market.
Comments		Gaining market share	Often used for FPGA transition	Losing market share

Example

Total cost calculation:



Comments

Market currently dominated by standard cell ASICs and FPGAs

- Ideally standard cell designs would be used for higher volume applications that justify the NRE

Many consider FPGAs separate from ASICs. Why?

- Different level of design skills required, especially in “back end” (place and route or physical design)
- Reduced level of verification required before “sending to factory”
- Again reduces sophistication required of team
- Low-cost (barrier) of entry
- Often different, lower cost Design Automation (CAD) tools
- Lower performance

However, front-end design (RTL coding) is virtually identical for each implementation style

Sometimes FPGA done first and standard cell ASIC done later

ASIC Design Flow

Major Steps:

1. High Level Design
   - Specification Capture
   - Design Capture in C, C++, SystemC or SystemVerilog (etc.)
   - HW/SW partitioning
   - IP selection (choose from pre-existing designs or “Intellectual Property”)
2. RTL Design
   - Major topic of this course
3. System, Timing and Logic Verification
   - Is the logic working correctly?

ASIC Design Flow

4. Physical Design
   - Floorplanning, Place and Route, Clock insertion
5. Performance and Manufacturability Verification
   - Extraction of Physical View
   - Verification of timing and signal integrity
   - Design Rule Checking

ASIC Design Methodology

Most ASICs are designed using a RTL/Synthesis based methodology

Design details captured in a simulatable description of the hardware

- Captured as Register Transfer Language (RTL)
- Simulations done to verify design

```
module LFSR_TASK (clock, Reset, Y1, Y2);

input        clock, Reset;
output [7:0] Y1, Y2;

reg    [7:0] Y1, Y2;

parameter [7:0] seed1 = 8'b01010101;
parameter [7:0] seed2 = 8'b01110111;

parameter [7:0] Taps1 = 8'b10001110;
parameter [7:0] Taps2 = 8'b10101110;

  task LFSR_TAPS8_TASK;

    input  [7:0] A;
    input  [7:0] Taps;
    output [7:0] Next_LFSR_Reg;

    integer N;
    reg Bits0_6_Zero, Feedback;

    reg [7:0] Next_LFSR_Reg;

      begin
        Bits0_6_Zero = ~| A[6:0];
        Feedback = A[7] ^ Bits0_6_Zero;
        for (N=7; N>=1; N=N-1)
          if (Taps[N-1] == 1)
            Next_LFSR_Reg[N] = A[N-1] ^ Feedback;
          else
            Next_LFSR_Reg[N] = A[N-1];
        Next_LFSR_Reg[0] = Feedback;
      end

  endtask /* LFSR_TAPS8_TASK */
```

Methodology (cont'd)

Automatic synthesis is used to turn the RTL into a gate-level description

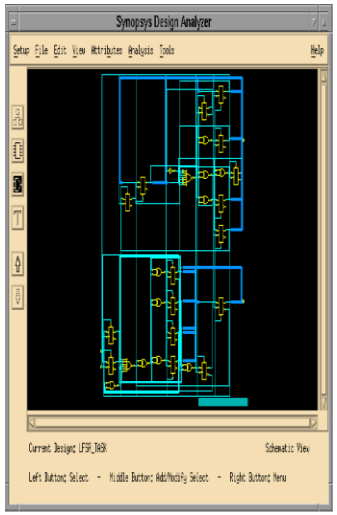
- ie. AND, OR gates, etc.
- Chip-test features are usually inserted at this point

Gate level design verified for correctness

Output of synthesis is a "net-list"

- i.e. List of logic gates and their implied connections

```
NOR2 U36 ( .Y(n107), .A0(n109), .A1(\value[2] ) );
NAND2 U37 ( .Y(n109), .A0(n105), .A1(n103) );
NAND2 U38 ( .Y(n114), .A0(\value[1] ), .A1(\value[0] ) );
NOR2 U39 ( .Y(n115), .A0(\value[3] ), .A1(\value[2] ) );
```



Methodology (cont'd)

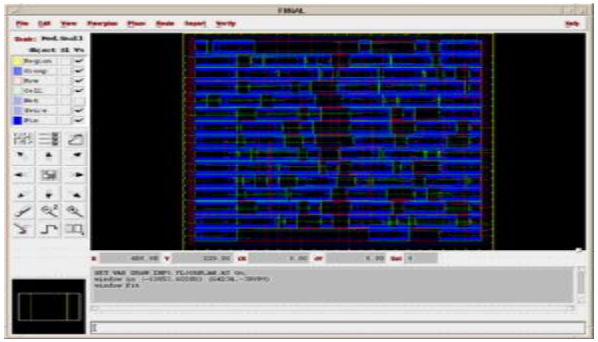
Physical Design tools used to turn the gate-level design into a set of chip masks (for photolithography) or a configuration file for downloading to an FPGA

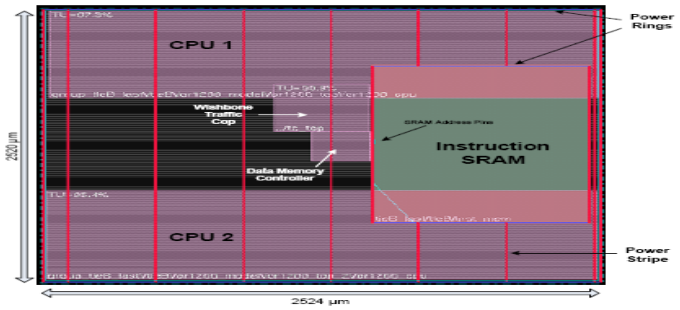
Floorplanning

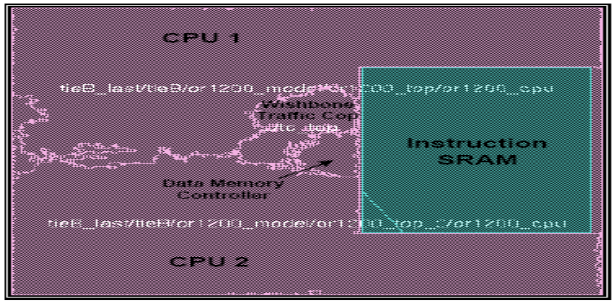
- Positioning of major functions

Placement

- Gates arranged in rows







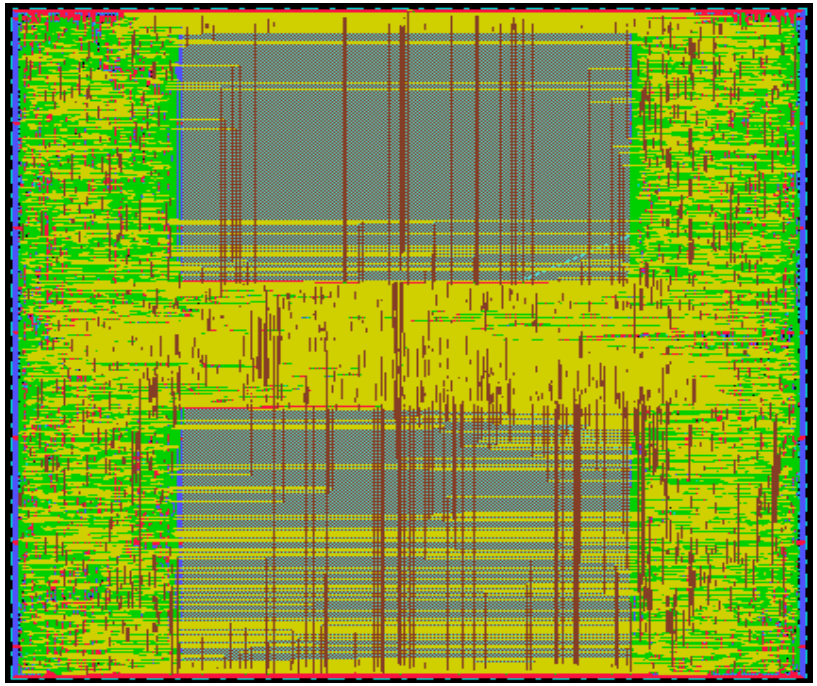
Methodology (cont'd)

Clock and buffer Insertion

- Distribute clocks to cells and locate buffers for use as amplifiers in long wires

Routing

- Logic Cells wired together

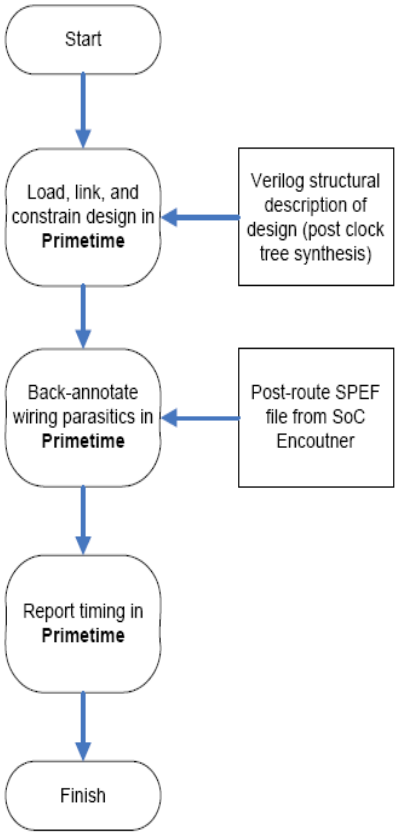


Methodology (cont'd)

Subflow example:

Timing Closure:

- "Front end" of design process
  - = Design capture, simulation and synthesis
  - Assumes abstract information about impact of wires
- "Back end" of design process
  - Place and route
  - Requires accurate wiring models



Future Issues

Increased cost of custom fab

- First chip run will cost over $2M for 90 nm
- Multiproject wafers

Increased cost of design

- Must be addressing > $1B market to justify a new chip run

Globalization

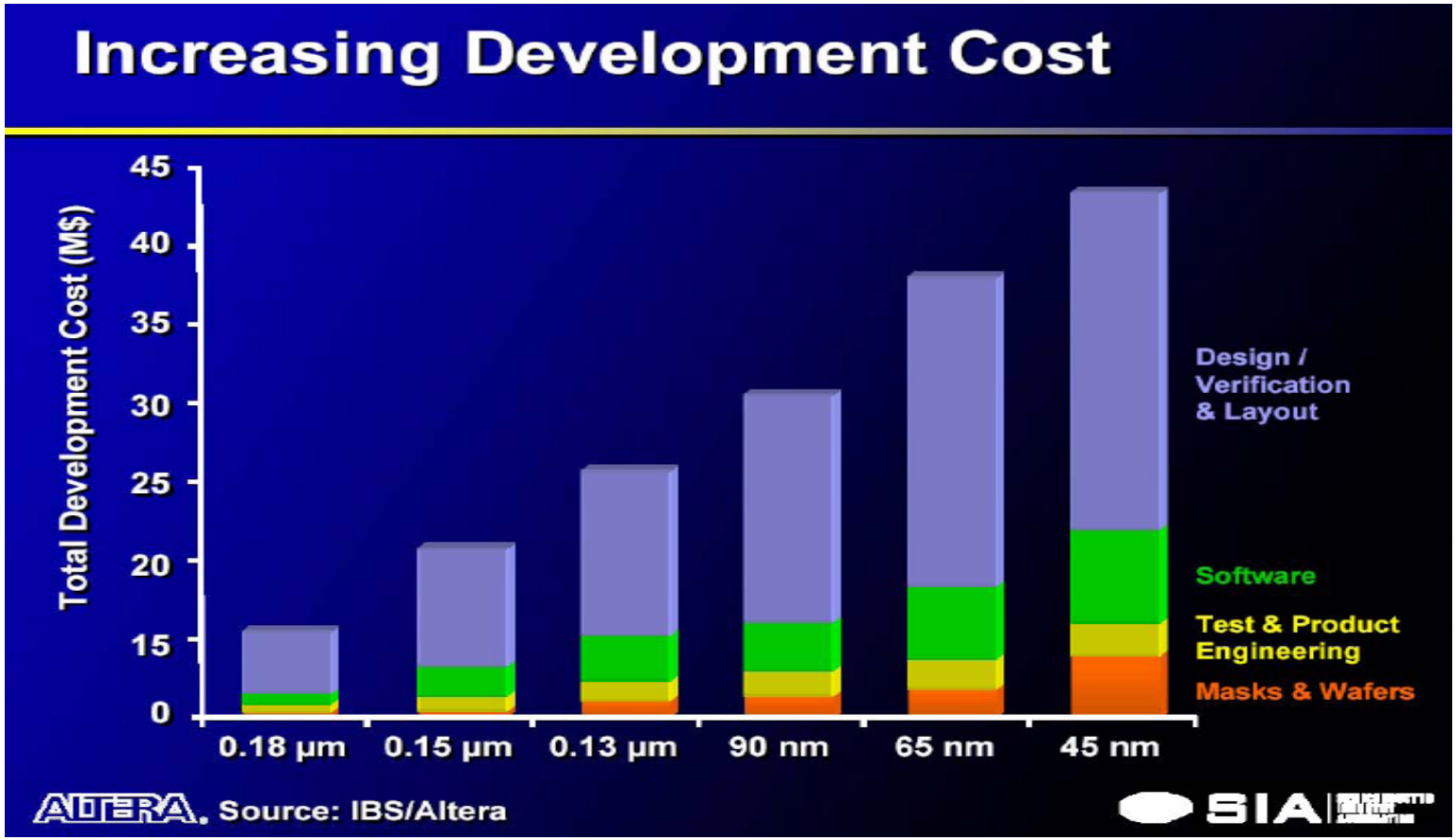
- Time-to-market and other competitive issues

Future Issues (cont'd)

Trends

- Increased use of FPGA and Gate Arrays
- Increased use of 'platform' solutions
  - Multi-core embedded CPU + ASIC accelerators
  - Configurable systems
  - Existing designs ('IP')
- Increased use of SystemVerilog, SystemC and other system modeling tools
- Complexity shifting from design to logical and performance verification
  - Logical verification = function; Performance = speed
- Cost to first silicon getting so high that the total addressable market must be very large and product risk low

Design Cost


Increasing Development Cost
Total Development Cost (M$)
45
40
35
30
25
20
15
0
0.18 µm
0.15 µm
0.13 µm
90 nm
65 nm
45 nm
Design / Verification & Layout
Software
Test & Product Engineering
Masks & Wafers
ALTERA
Source: IBS/Altera
SIA

Questions

- What basic technological trend drives the Semiconductor Industry?
- What is the key difference between a standard cell ASIC and an FPGA?
- What will be important challenges to future design houses?
- What is a “fabless semiconductor vendor”?

Summary

Over the next ten years, product growth will be driven by:

- Underlying technology push
- High demand for graphics, multimedia and wireless connectivity
- Insidious insertion of electronics and computers into our everyday lives

Many of the resulting products will require specialized silicon chips to meet performance (speed/size/weight/power/cost) demands – ASICs

ASIC design methodology includes logic, timing, and physical design

- Unfortunately, design productivity is not keeping up with chip performance growth

Summary (cont'd)

To match this product need, the capability of a silicon CMOS chip will continue doubling every 2-3 years until after 2015.

- To sell a product at $300-$1,000, it can only include one high value chip
  - Thus product performance is determined by the performance of that one chip
- AND talk about planned obsolescence!!

ASIC styles include full custom (for analog) and RTL-based design: Cell based (semi-custom), Gate Array or FPGA implementation