Application Report
SPRA550

3.3V DSP for Digital Motor Control

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Abstract

New generations of motor control digital signal processors (DSPs) lower their supply voltages from 5V to 3.3V to offer higher performance at lower cost. Replacing traditional 5V digital control circuitry by 3.3V designs introduce no additional system cost and no significant complication in interfacing with TTL and CMOS compatible components, as well as with mixed voltage ICs such as power transistor gate drivers. Just like 5V based designs, good engineering practice should be exercised to minimize noise and EMI effects by proper component layout and PCB design when 3.3V DSP, ADC, and digital circuitry are used in a mixed signal environment, with high and low voltage analog and switching signals, such as a motor control system. In addition, software techniques such as Random PWM method can be used by special features of the Texas Instruments (TI™) TMS320x24xx DSP controllers to significantly reduce noise effects caused by EMI radiation.

This application report reviews designs of 3.3V DSP versus 5V DSP for low HP motor control applications. The application report first describes a scenario of a 3.3V-only motor controller indicating that for most applications, no significant issue of interfacing between 3.3V and 5V exists. Cost-effective 3.3V-5V interfacing techniques are then discussed for the situations where such interfacing is needed. On-chip 3.3V analog-to-digital converter (ADC) versus 5V ADC is also discussed. Sensitivity and noise effects in 3.3V and 5V ADC conversions are addressed. Guidelines for component layout and printed circuit board (PCB) design that can reduce system's noise and EMI effects are summarized in the last section.

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Introduction

To be cost competitive, new generations of digital signal processors (DSPs) must shrink the physical size of internal circuitry to achieve higher integration levels. This has been an industry trend all along. For example, the gate oxide of transistors on the most advanced DSPs has reached 0.18 microns; only a few years ago, the same geometry was at 1.0-micron level. Smaller geometry allows more circuits to be packed more closely together. This not only increases the level of integration, but also shortens the travel distances for electrons; therefore, shrinking increases the speed and level of integration at the same time. Higher level of integration means lower cost.

In order to restrict voltage stress on the thinned out transistor oxide, the supply voltages must naturally be lowered. This gives rise to 3.3V motor control DSPs. Lowering the supply voltage to a component brings down power consumption by the component when the component is clocked at the same frequency. This applies to any circuit component, including the DSP. Reduced power consumption directly translates into reduced component size for the on-board power supply and reduced system cost.

There is a wide range of 3.3V compatible components and ICs in the market. As a result, the off-chip peripherals in a typical motor controller can usually be obtained in 3.3V. So the entire logic portion of a motor controller may run at 3.3V plus the commonly required 15V gate voltage for power transistors. However, there may be situations where 5V components or ICs are still used along with a 3.3V DSP. This could be due to design legacy of a specific motor control application. The workaround is simple and inexpensive. Even in cases where level shifters such as FETs are needed, the statement is still true. Typically there are only few input/output (I/O) pins of the processor that may require such level shifters.

The *3.3V-Only Motor Controller* section of this application report discusses the case where only 3.3V and 15V components are used in the motor controller design. Examples are given for 3.3V peripheral components that typically interface with a DSP controller device.

The *Interfacing to DSP Inputs* section and *Interfacing to DSP Outputs* section present different options of 3.3V-5V interfacing techniques with recommended circuits. The *Interfacing to DSP's ADC Inputs* section addresses the noise concerns related to 3.3V on-chip ADC, indicating that the noise issue for a 3.3V converter is not necessarily different or worse than that of a 5V ADC in many applications. It is also indicated that software techniques such as over-sampling and random pulse-width modulation (PWM) can be applied to significantly reduce noise and EMI effects, which would improve conversion results. These techniques can be readily implemented in a design with the CPU performance and special features of TMS320x24xx DSP controllers. General considerations regarding the noise and EMI reduction of PCB design and layout are discussed in *Power Supply and General PCB Design Considerations* section.

3.3V-Only Motor Controller

A DSP motor drive system typically consists of input power supply stage, power inverter including power transistors and their gate drivers, DSP controller, and a motor that is controlled by the controller. There are also logic components that interface with the DSP for functions such as sensing and communication. Figure 1 shows the block diagram of a basic DSP motor drive system, with the high and low voltage blocks separated by dashed lines. Input power supply stage rectifies AC input line and provides DC voltage (DC Bus Voltage) for the switching power transistors in the inverter that deliver energy to the motor. The on-board power supply circuits provide the 15V needed by the gate drivers and 3.3V (and 5V if necessary) needed by digital logic. The circuits usually consist of a transformer or DC-DC converter, and a voltage regulator. 3.3V circuitry consumes less energy than equivalent 5V circuitry at same frequency. Therefore the transformer or DC-DC converter can be smaller when 3.3V DSP and components are used in a motor drive.

There are usually only a few types of peripheral circuits and components that interface to the DSP. The following are the most common examples:

- Communication interface for SCI (serial communication interface) and CAN (control area network) controller such as RS-232 and CAN transceiver
- Serial components connected to SPI (serial peripheral interface) such as serial DAC, serial EEPROM, and serial LED driver
- Power device (IGBT or MOSFET) drivers for the PWM outputs
- Voltage and current sensing and conditioning circuits that interface to the on-chip ADC
- Speed and position sensing sensors that interface to the capture and quadrature-encoded-pulse (QEP) decoding logic such as hall-effect sensors and optical encoders

These peripherals, except for the driver circuits that are typically 15V, are mostly available in 3.3V or 3.3V compatible forms and have no issue interfacing directly to a 3.3V DSP.

The driver circuits typically require a higher supply voltage. It is the inputs of these drivers that interface with the PWM outputs of the 3.3V or 5V DSP. However, the PWM output level and current capability of TI's 3.3V DSPs are compatible with the typical driver ICs such as IR210x that are available on the market. Therefore, it is very likely that the entire motor controller would only need 3.3V DC supply in addition to the 15V DC supply. Table 1 gives a list of example 3.3V or 3.3V-compatible circuit components that interface to a motor control DSP. A CAN transceiver is not available in 3.3V today. The interfacing circuits discussed later in this application report can be used to interface with any available CAN transceiver.

Figure 1. Block Diagram of a Typical DSP Motor Controller

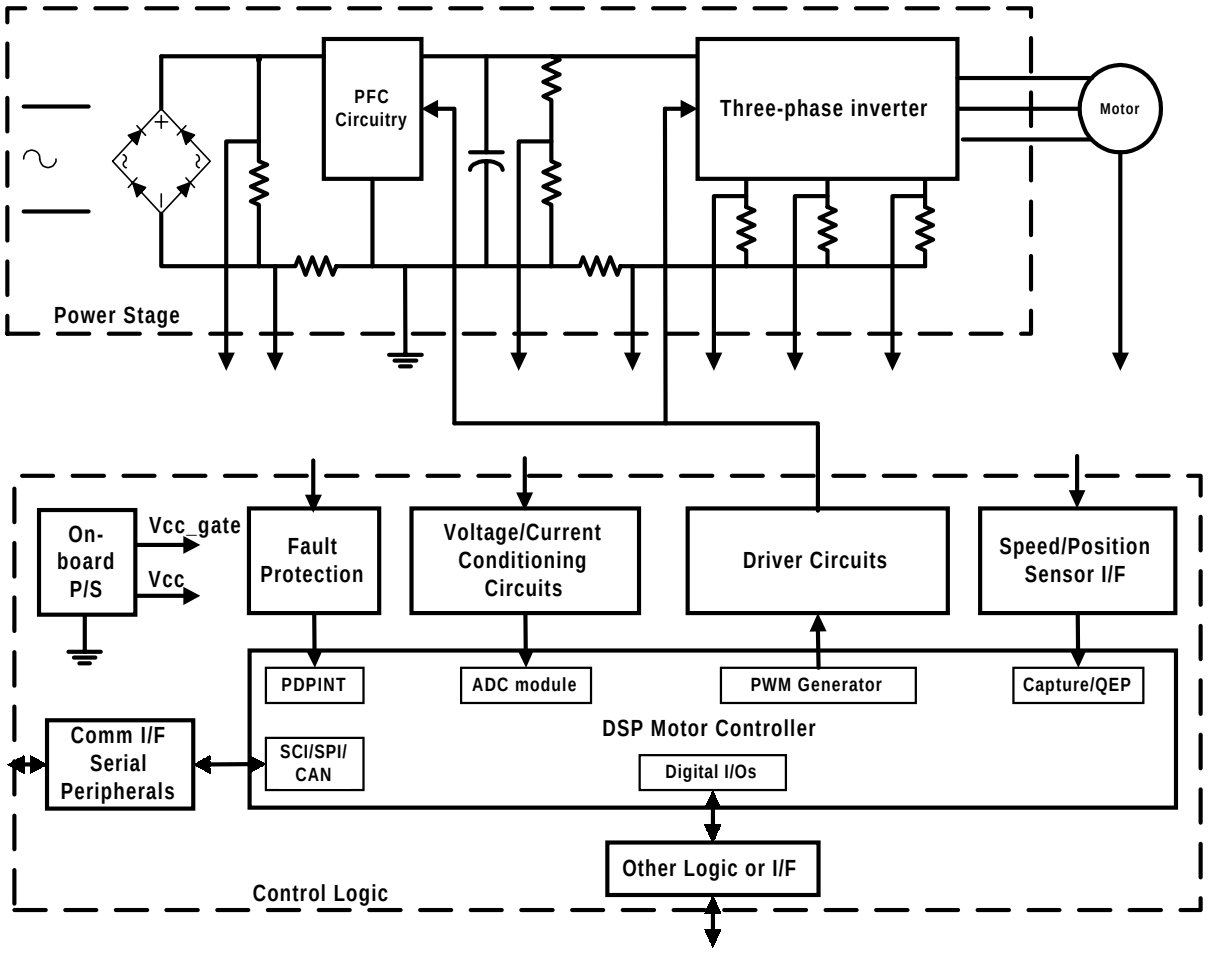


Table 1. Availability of 3.3V Peripheral Components

DSP module	Peripheral Components	3.3V Examples of Peripheral Components	Comment
SCI	RS-232 transceiver	TI SN75LV4737A (3/5) Maxim MAX3221 (1/1), MAX3223 (2/2)	Numbers in brackets: number of receivers/number of transmitters
SPI	Serial DAC	TI TLA5604(4 10-bit), TLA5614(4 12-bit), TLS5616(1 12-bit)	First number in bracket indicates number of channels
	Serial EEPROM	Microchip 25AA040/080/160/320/640 (4-64K bits) 25LC040/080/160/320/640 (4-64K bits)	These are SPI compatible serial EEPROMs
CAN	CAN Transceiver	Not available	See interfacing techniques.
PWM	IGBT/MOSFET driver	IR210x IR210x4	These are 15V parts, but directly interface to 3.3V DSP
A/D	Operational Amplifier Resistor divider and filter	TI TLC27x, TLV27xx, TLV22xx, TLV24xx, TLV246x	Resistor divider interface to 3.3V DSP is straight forward
Capture/QEP	Hall-effect sensor Opto-isolator	Hall sensors with open-collector output or without output amplification Most opto-isolators	3.3V op-amp circuit can be used for hall sensor without output amplification
Supply voltage	Supply voltage regulator	TI TPS7233 (100mA), TPS7133(500mA), TPS7333(500mA with LVD), TL5001A(1A)	TI TPS73HD301 (750mA per output) is an available dual 3.3V-5V regulator
Supply voltage monitoring	Supply voltage supervisor	TI TPS3823-33, TPS3824-33, TLC7733	TI TPS3305-33 is an available dual 3.3V-5V supervisor
I/O	Standard logic MOSFETs Opto-isolator	TI Standard LVC, ALVC, LVCT LVT, ALVT, HC, AHC, AC families Most opto-isolators 3.3V MOSFETS	LVC, ALVC, LVT, ALVT and AHC logic operate at 3.3V Vcc and accept 5V input. LVT and ALVT families are TTL compatible.

Interfacing to DSP Inputs

Although it is possible to have a fundamental motor controller that is completely 3.3V, there are indeed situations where interfacing between 3.3V and 5V can not be avoided. Several different types of interface situations to the DSP input pins are presented in the following.

DSP input pins sometimes have internal pull-up or pull-down circuits. These circuits approach ideal current sources given a fixed V_{cc}. As such, they will not affect impedance calculations (RC time constants) for the interface circuitry; however, they can substantially affect DC bias. Be sure to check the device-specific data sheet for information on pin pull-up and pull-down and rated current before making bias calculations. The following examples do not take into account the internal pull-ups or pull-downs to simplify the discussion.

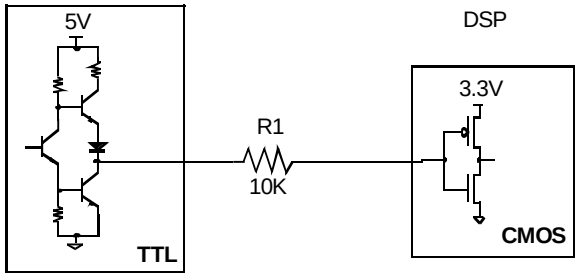
5V TTL Output to 3.3V DSP CMOS Input

The high output voltage level (V_{oh}) of TTL output is typically 3.4V at rated current, and 4.05V at no-load, when supplied with maximum supply voltage of 5.25V (V_{cc5_max}). The tolerable high input voltage (V_{ih}) of 3.3V DSP is (V_{cc3} + 0.3V), where V_{cc3} is the 3.3V supply. Since we must assume the worst-case differential voltage between the devices, we set V_{cc3} = 3.0V, thus the maximum differential voltage for logic high is 0.75V.

If you want to limit the current to 75uA, then placing a 10K-ohm resistor between the TTL output and 3.3V CMOS input will suffice. This creates a small typical RC delay of about 10K × 5pF = 50nS. This delay should be negligible in any case except perhaps CAN (or J1850) transceivers that are subject to a maximum round-trip time. Higher resistance values can be used to limit the current further down. However, the delay becomes bigger and noise immunity gets worse as the resistance value goes up. The interface technique shown in Figure 2 interfaces a 5V TTL to 3.3V CMOS that can be used, if current limit is an important concern.

This same technique will work for an open-emitter pull-up, except that the falling time constant will be longer considering that there is now a transistor emitter capacitance to deal with.

Figure 2. 5V TTL Output to 3.3V DSP CMOS Input



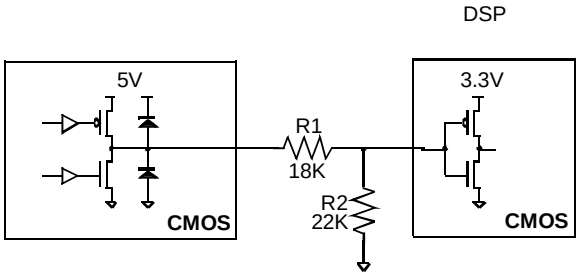
5V CMOS Output to 3.3V DSP CMOS Input

Using the same analysis as previously discussed, the V_{oh} level of 5V CMOS outputs is typically 5.25V at no-load and a V_{cc5_max} of 5.25V. The maximum differential voltage for logic high is, therefore, 1.95V, which presents a slightly more difficult problem. In this case, you need to add a resistor divider network (Figure 3), such that a signal voltage level of 5.25V appears at the input of DSP as 3.0V. Since the divider is referenced to ground, a 0V signal appears as 0V at the DSP input.

Using the same argument from the previous section that a 10K ohm source impedance yields an acceptable time constant, you can select the two resistors of the divider to be R_1 = 18K and R_2 = 22K. Using these values, a 5.25V output voltage of an off-chip component yields a 2.9V voltage level at the DSP CMOS input. The I_{oh} current will be limited to 130uA and the impedance seen by the DSP CMOS input will be 9900 ohms. The resistance values can be smaller if the current limit is set to a higher value, resulting in a lower source impedance value.

This technique will work exactly the same for an open-source pull-up, except that the falling time constant will be longer considering that there is now a transistor drain capacitance to deal with during fall time.

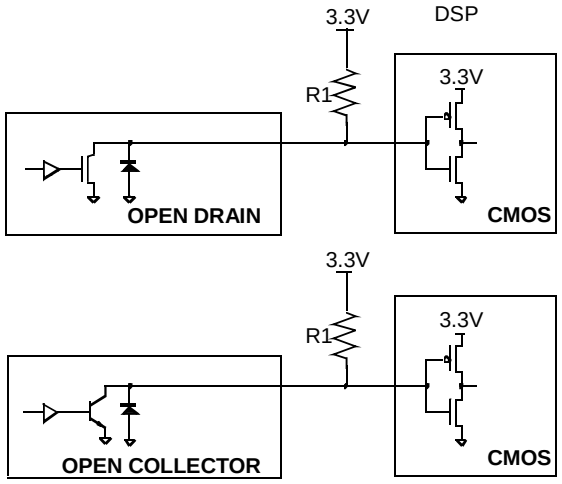
Figure 3. 5V CMOS Output to 3.3V DSP CMOS Input



Open Drain/Open Collector Output to 3.3V DSP CMOS Input

This is not a 3.3V-to-5V interfacing issue (unless the output has to be pulled up to 5V, which usually should not be the case). However, it exists as a general interfacing problem in typical applications. This type of input requires a pull-up resistor to the 3.3V power rail (Figure 4). Considering the significant increase in capacitance, $C_{junction}$, due to the drain/collector junction, the rise time, $T_r = R_{pu} * (5pF + C_{junction})$, will be slowed unless the pull-up resistor is reduced from the usual 10K ohms.

Figure 4. Open Drain/Open Collector Pull-Down to 3.3V DSP CMOS Input



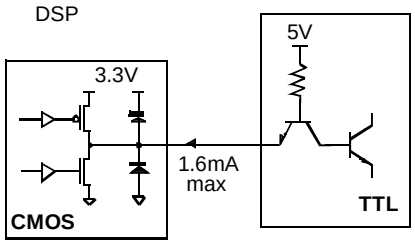
Interfacing to DSP Outputs

Like the inputs, outputs may need translation to other technologies or voltage levels. Following are examples of various output interfaces.

3.3V DSP CMOS Output to 5V TTL Input

As the DSP outputs are TTL compatible, no special circuitry is required. The V_{ih} and V_{il} for TTL are 2.4V and 0.8V, respectively; this gives plenty of margin to the 2.8V to 0.4V swings of the 3.3V CMOS output buffer (Figure 5). Inputs of many motor control components are TTL compatible. Although they may need a 5V supply, they interface to a 3.3V DSP directly. Many MOSFET and IGBT drivers derive the 5V supply internally from the 15V that is needed to guarantee a typical 15V-output level.

Figure 5. 3.3V DSP CMOS Output to 5V TTL Input

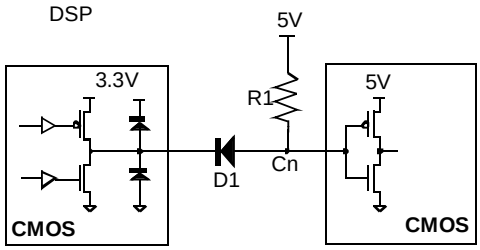


3.3V DSP CMOS Output to 5V CMOS Input

Going from 3.3V DSP CMOS output to 5V CMOS input requires level shifting. In Figure 6, R_1 and D_1 provide a 0.6V upward shift of the CMOS output's voltage. With R_1 around 10K ohms, the CMOS output buffer swings from about 0.2V to 3.3V. At the diode's anode, it swings from about 0.8V to 3.9V. The 5V CMOS input thresholds are 1.0V and 3.5V, which gives 0.2V and 0.4V of margin, respectively. Here, there is a small rise-time delay due to the RC time constant of R_1 and the node capacitance, C_n.

Some IGBT or MOSFET drivers require a 5V CMOS input level; therefore, the circuit in Figure 6 is needed to interface the DSP to such drivers.

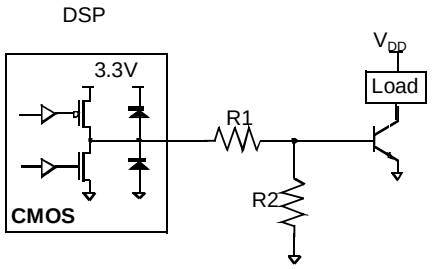
Figure 6. 3.3V DSP CMOS Output to 5V CMOS Input



3.3V DSP CMOS Output to Bipolar Input

The circuit shown in Figure 7 is the same whether the output driver is 3.3V or 5V. However, the resistors need to be resized to match the lower V_{oh} to the required base drive current and maintain the required current gain.

Figure 7. 3.3V DSP CMOS Output to Bipolar Input

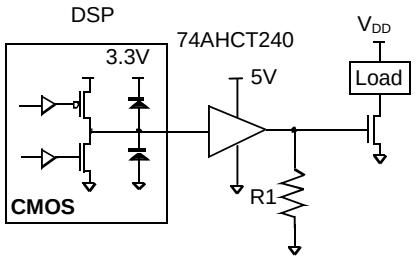


3.3V DSP CMOS Output to MOSFET Input

This is the most challenging of the conversions (Figure 8). Many MOSFETs available require more than 3.3V on their gate to saturate at the required load current. Newer MOSFETs with less restrictive specification are slowly becoming available.

One low-cost technique is to use a standard 5V CMOS buffer such as the 74HCT04 (or 74AHCT04) hex inverter or the 74HCT240 (74AHCT240) octal buffer to translate the 3.3V CMOS output up to a 5V CMOS level. The 74HCT04's are available in industrial temperatures for less than $0.15 each at high volume and one device will translate 6 outputs. Note that, in this implementation, R1 is a gate pull-down for safety purposes.

Figure 8. 3.3V DSP CMOS Output to MOSFET Input



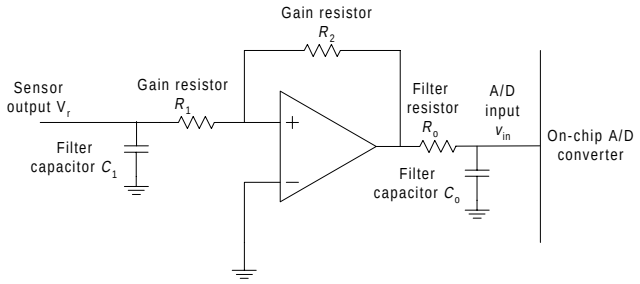
Interfacing to DSP's ADC Inputs

It is as important to 3.3V ADC as it is to 5V ADC, that good engineering practice be excised to minimize system noise levels. In this section, software and hardware techniques related to ADC in typical motor control applications are discussed. Fractional horsepower (HP) motor drives are assumed here that are widely used in many consumer and industrial products. The goal here is to examine factors and techniques that will reduce effective noise by software and hardware techniques at practically no extra cost. Toward that goal, we provide some guidelines to consider:

- What can be done in control design and software algorithms when using high performance DSP controller with fast on-chip ADC
- What can be done in hardware design and PCB layout to reduce effects of noise

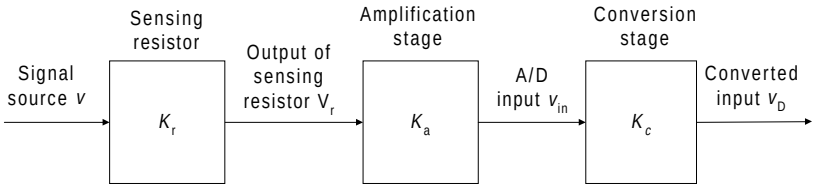
Figure 9 is an illustration of a typical circuit that interfaces to ADC input. For simplicity, the level-shifting circuit that is often needed to convert a bipolar signal into a unipolar signal is not shown in the figure. For motor control applications, typical signal sources are DC bus voltage, motor phase current, and motor phase voltage. Current-sensing resistors and voltage-divider resistors, as shown in Figure 1 of *3.3V-Only Motor Controller* section, are typically used to sense these quantities. If the sensor output is within the 0 to 3.3V or 0 to 5V input range of the ADC, with no significant noise, and meets the source impedance requirement of the ADC, direct connection between the sensor output and ADC input can be made. In the case of voltage sensing, proper selection of divider resistor values can usually produce the right input swing. However, in either case, an op-amp amplifier circuit as shown in Figure 9 may also be used to assure proper range of analog voltage swing, provide signal smoothing and filtering, and meet input impedance requirement of the ADC.

Figure 9. Typical ADC Interface Circuit for DSP



The signal path of A/D conversion is shown in Figure 10. For 3.3V ADC, the sensing and amplification stages usually must produce at the ADC input a signal swing of 0-3.3V (similar to the 0-5V range for 5V ADC). This is to achieve maximum signal magnitude and signal-to-noise ratio at the ADC input. Therefore, the gain, K_rK_a, for a 3.3V converter is 3.3/5 times smaller than that for a 5V converter. The conversion stage carries out the analog-to-digital conversion. The range of conversion result for a 3.3V converter and 5V converter is the same, which is 0-1023, when the resolution is both 10 bits. However, 1023 corresponds to 3.3V input for a 3.3V converter and 5V input for a 5V converter. Therefore, the gain for this stage, K_c, for a 3.3V converter is 5/3.3 times larger than that for a 5V converter.

Figure 10. A/D Conversion Signal Path



Noise Considerations

Noise in the ADC result comes from noise at the signal source, noise injected at the sensing resistor and between the sensing resistor and the op-amp, and noise injected at the op-amp and between the op-amp and the ADC input.

Noise at the signal source is subject to gain K_rK_a before appearing at the input of the ADC. Since the gain for this noise of a 3.3V converter is 3.3/5 times smaller, the effective magnitude of this noise at the ADC input is 3.3/5 smaller. However, because the conversion gain K_c is exactly 5/3.3 times larger, the effects of this noise are brought back to the same level in the conversion result.

Noise injected at the sensing resistor and between the sensing resistor and the op-amp is subject to gain K_a before appearing at the input of the ADC. The total effective gain for this noise is K_aK_c. Although K_c is 5/3.3 times bigger for 3.3V ADC, K_a for 3.3V ADC is typically 3.3/5 times smaller to scale the signal from 0-5V range to 0-3V range. Therefore, the total effective gain for this noise is usually the same between 3.3V ADC and 5V ADC.

Overall, the effects of noise injected before the amplification stage remains the same between a 3.3V converter and a 5V converter.

Noise injected at the amplification stage and between the amplification stage and the DSP is coupled directly into the input of the DSP. Since the gain for the conversion stage is 5/3.3 times larger, the effects of this noise is 5/3.3 times higher for a 3.3V converter when compared to a 5V converter. However, having the DSP and all digital logic running at 3.3V instead of 5V should generate less noise contribution between the output of the op-amp and the ADC pin. At the same clock frequency, noise contributed by digital logic is reduced by a factor of $(3.3/5)^2$ in terms of power density.

Overall, noise considerations are important to digital motor control applications whether at 3.3V or 5V. The following are a few hardware and software techniques that aim at resolving the noise issue, followed by a section on PCB and layout considerations that can be taken to reduce the effects of noise.

Decoupling/Bypassing Capacitors and Pull-up and Pull-down Resistors

As a generally known practice, decoupling or bypassing capacitors placed near the source and power supply terminals greatly reduce noise propagation. Pull-up and pull-down resistors for unused DSP inputs avoid current draw by internal circuits caused by floating inputs; thus reducing noise generation. Having a small loading resistor (such as 50 ohms) on the high-frequency output also helps reduce peak transient currents and associated noise generation.

Low-pass Filter

A significant amount of noise comes from events correlated to switching of power devices for pulse-width modulation (PWM) that are known to generate high dv/dt and di/dt. Since the frequency of this kind of noise is usually much higher than the frequency range of the useful signal, R-C filters with proper cut-off frequencies can usually take out this kind of noise very effectively. The filter at the op-amp output in Figure 9 is a low-pass filter. The resistor in series must be carefully chosen, to match the impedance requirement of the ADC, and along with the filter capacitor to provide the correct cut-off frequency. This also helps stabilize the op-amp preventing noise generation because of instability of the op-amp circuitry. The filter capacitor also helps balance the switching transient and charging and discharging of the internal sample and hold capacitor during sample and hold. In addition, digital filters with a properly selected cut-off frequency can be implemented in the DSP controller to take out certain correlated and uncorrelated noise. The CPU bandwidth of a DSP certainly gives enough CPU room to implement any digital filter.

PWM Techniques

Asymmetric PWM technique switch all PWM channels at one end of every PWM period. In contrast, a symmetric PWM waveform is symmetric with respect to the middle of a PWM period. Therefore, symmetric PWM techniques generate less switching noise than asymmetric PWM techniques. Symmetric space-vector PWM techniques, such as the one implemented by on-chip hardware, reduce the number of power devices switching by 1/3; thus greatly reducing switching noise generation. In comparison to classical sinusoidal PWM techniques, space-vector PWM generates about 15% higher output voltage with the same DC bus voltage. Therefore, when output power is the same, lower current is generated by space-vector PWM, resulting in lower di/dt.

Random PWM techniques spread the power spectrum of PWM signals over the frequency variation range. This eliminates the effects of noise concentration in the power spectrum at the fixed carrier frequency and its multiples. The DSP controllers provide flexible peripherals and plenty of CPU bandwidth to implement randomized space-vector PWM.

Oversampling

Oversampling techniques as described in Reference 8 can be used to increase SNR or effective resolution of ADC results. Satisfactory implementation of oversampling to improve ADC resolution requires a fast ADC to sample analog inputs at a very high rate and a high-speed DSP to execute quality low-pass filtering and decimation. DSP controllers readily exceed both requirements. One advantage gained going from 5V DSP to 3.3V DSP controller is that the new 3.3V on-chip ADC of 3.3V DSP controllers (TMS320C240x) is almost two times faster than that of the 5V DSP controllers, while the CPU speed has increased by 50% (from 20 MIPS to 30 MIPS).

Table 2 shows improvement achieved by proper oversampling and processing in terms of SNR and effective bits of resolution. For many fractional to 1 HP applications, the bandwidth of motor current is usually 1-2KHz and the bandwidth of motor voltage or DC bus voltage is usually in the 100-200Hz range or lower. Taking current measurement as an example and assuming the bandwidth of motor current is 1.25KHz, then a 20KHz sampling of the current followed by proper software low-pass filtering can improve the SNR by 12dB, or equivalently increasing the ADC resolution by 2 bits.

Random noise is assumed for the results in Table 2. Otherwise, appropriate uncorrelated signals may be generated by the on-chip features of the DSP controller (such as PWM output filtered by RC circuit) and can be added to the ADC input to satisfy the oversampling assumption. The low-pass filter of the digitized signal can be carried out by the DSP controller using a moving average filter (for example, a FIR).

Table 2. Improvement of SNR and Bit Resolution with Oversampling

Oversampling factor p	SNR improvement in dB	Extra resolution in number of bits
2	3	0.5
4	6	1.0
8	9	1.5
16	12	2.0
32	15	2.5
64	18	3.0

Power Supply and General PCB Design Considerations

Designing for low noise and EMI from the start of a project results in an easier and less expensive solution than attempting to fix noise and EMI problems after a design has reached the testing phase of development. Consequently, following are a few guidelines for PCB design at the beginning of a project that can help to minimize noise and EMI effects, while adding little or no cost to the system.

PCB design guidelines for reduced noise and EMI are explained in details in references 9, 10, 11, 12, and 13. Provided here is a summary of some major points.

Sources of noise and EMI are:

- high- and low-power analog and switching circuits
- motors, power supplies and regulators, clock and crystal circuits
- digital processor high-frequency system clock and switching at its inputs and outputs

Any signal coming out of a source has a return path or ground. Path of travelling and return signal forms a loop that can operate as radiating (or receiving) antennas for EMI and noise coupling onto other components and loops. Signal traces on the PCB form loops of various areas. Strength of the EMI noise depends on the square of frequency of the travelling signal, current flowing in the loop, and the loop area. Differential-mode and common-mode noise are also present on the PCB and depend on the signal loop and the system ground, and its potential levels at different nodes.

Following is a summary of PCB design guidelines to reduce noise and EMI effects:

- PCB floor-plan
  - Analog, digital, and noisy components should be located on the PCB by category (that is, localized and separate from each other).
  - Allow space for grounding.
  - Minimize routing distances.
  - IC's that have high-frequency signals (more than 50KHz) should be placed near each other to minimize routing distances of clock and fast signals.
- Grounding
  - Digital: Grid the ground. Ground grid provides a low-impedance signal return path that resembles that of a 4-layer board using ground plane. This works very well with 2-layer boards.
  - Analog: Use parallel grounding scheme for sensitive analog circuitry and use series grounding scheme for less sensitive analog circuitry. Power should be routed over (under) or next to ground whenever possible in order to minimize radiating loop areas for high-frequency noise signals.

    In a motor drive PCB system, use fat tracks for the high di/dt DC bus rails and phase outputs of an inverter. Run the gate signals in parallel to the corresponding source of MOSFET or IGBTs. Use appropriate gate resistors to protect the driver outputs. Sometimes, decoupling capacitors between the DC bus rails are needed to cancel stray inductance.
  - Noisy: Isolate analog from digital grounds. Noisy grounds support circuitry that generates a significant amount of ground bounce, such as relays and motors. This ground should be isolated from digital and analog grounds (such as DSP-ADC's) in order to keep high levels of ground noise away from analog and digital circuitry. In a mixed-signal environment, a digital and analog ground should be connected near or under the digital processor, and these grounds should be connected to the noisy ground near the signal path connection.
  - Low impedance ground node: Connect digital, analog, and noisy grounds together at the lowest impedance ground node on the PCB. Ground traces should be as wide as possible in order to provide lowest resistance path for current.
  - Connectors: Provide low-impedance ground between IC's and connectors.
  - Fast signals: Run digital ground next to fast signals (or over if possible).
  - Avoid routing signals, especially fast signals, under other components.
  - Provide localized digital ground plane, placed under the digital processor to provide shielding.
- Bypassing
  - Power: Capacitors should be located as near as possible to digital and analog voltage supply and ground/return pins. Supplies should be bypassed to their own ground/return nodes.

- Signal: Capacitors should be located as near as possible to the associated pins. Bypass capacitors can be placed on the bottom side of the board directly underneath the VCC/VSS pins.
- Connectors: Proper grounding between the digital processor and a connector is necessary for the bypass capacitors at the connector to prevent noise on the wiring harness.

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